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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,454	07/17/2002	Kuang-Kai Kuo	8327-US-PA	5796

31561 7590 04/15/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
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EXAMINER	
ROSS, JOHN M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 04/15/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,454	KUO ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/5/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claim 7 is canceled.

Claims 1-6 and 8-11 are pending in the application.

Claims 1-6 and 8-11 are rejected.

Response to Amendment

2. Applicant's amendment filed on 5 February 2004 (Paper No. 4) in response to the office action mailed on 3 November 2003 necessitates new ground(s) of rejection under 35 USC 103(a) applied to claim 11 as presented below in this Office action.

Applicant's arguments regarding the remaining claims have been fully considered, but they are not persuasive. Therefore, the rejections made under 35 USC 103(a) in the previous office action are maintained and restated below.

Drawings

3. The drawings filed on 5 February 2004 have been approved by the Examiner.

Specification

4. The disclosure is objected to because of the following informalities:

Amendment A provides a substitute for paragraph [0018], however, the substitution should have been made for paragraph [0021]. Applicant is required to restore the original paragraph [0018] and substitute the new paragraph for paragraph [0021].

Claim Objections

5. The amendment has overcome the objections to the claims.

Claim Rejections - 35 USC § 112

6. The amendment has overcome the rejections under 35 USC 112.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 5-6, 8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379) in view of Mills (US 5,497,355) and Pollak (US 6,618,724).

As in claim 1, Becker describes a memory control system coupled to a system bus (Figs. 1 and 5a, elements 12 and 22; column 3, lines 11-16 and 30-33) and having a clock line (Figs.

3a-3c, element labeled "CLK"; column 6, lines 28-38), where the memory control system comprises:

a memory write command queue for holding a plurality of memory write commands, wherein each said memory write command has an address (Fig. 5a, elements 90 and 92; column 8, lines 53-57);

wherein the memory control system receives a read address of a read command (i.e. a memory read operation) according to a clock signal (Fig. 1; column 4, lines 31-36; Figs. 3b-3c; column 6, lines 43-62; column 8, lines 1-17);

a memory request organizer function wherein the read address is compared with the write address of each memory write command in the memory write command queue, and if the comparison indicates the presence of identical bits, the execution of the memory read command is delayed until the matching memory write commands in the memory write command queue execute (Column 9, lines 1-9; column 12, lines 19-35); and

wherein if the comparison indicates a difference, execution of the memory read command is permitted (Column 12, lines 63-66).

Becker does not teach that the read address is received sequentially by a bus interface unit as a first and second section, and that the first and second sections are output concurrently, as required by claim 1.

Mills teaches an address demultiplexer coupled to a memory request bus (i.e. a bus interface unit) where an address is received sequentially as a row address (i.e. first section) and column address (i.e. second section), and the row and column addresses are output concurrently (Fig. 5, column 13, lines 3-13). Mills teaches that this arrangement allows synchronous address latching circuitry to work with multiplexed addresses such as those occurring in dynamic random access memories (Column 12, lines 57-60).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the address demultiplexing arrangement taught by Mills, in the system of Becker, in order to allow synchronous address latching circuitry to work with multiplexed addresses as taught by Mills.

The combination of Becker and Mills does not teach a two-step comparison algorithm where the first section read address is first compared, and the second section read address is compared if the first section read address indicates a match, as required by claim 1.

Pollak teaches a string comparison algorithm where characters comprising identical bit portions of two strings are compared such that if the first characters match (i.e. first section), the second characters (i.e. second section) are subsequently compared, but if the first characters do not match, the comparison is terminated and execution of a controlling process continues (Fig. 2, column 4, lines 18-39). It may be understood from the teaching of Pollak that by stopping the

comparison after the first mismatch is found, the time required to compare the strings is less than if the entire strings were compared (Column 1, line 66 to column 2, line 4).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to compare the read address as a series of subsequent comparisons on a first and second section of the read address as in the comparison algorithm taught by Pollak, in the system made obvious by the combined teachings of Becker and Mills, due to the similarity in the nature of the problems to be solved, namely the comparison of unitary collections of bits, and in order to reduce the time required to make the comparison as taught by Pollak.

Regarding claims 5-6, although the combination of Becker, Mills and Pollak does not teach that when comparing the first and second sections of the read and write addresses, the first section of the address includes bits 12 to 31, and that the second section of the address includes bits 6 to 11, such limitations are merely a matter of design choice and would have been obvious in the system of Becker, Mills and Pollak. Becker, Mills and Pollak teach a comparison made between the first sections of a read and write address, and a comparison made between the second sections of a read and write address. The limitations in claims 5-6 of the instant application do not define a patentably distinct invention over Becker, Mills and Pollak since both are directed toward comparing addresses that are divided into two distinct portions. The particular assignment of bit ranges to these portions is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to assign bits 12 to 31 as the first section of the address, and to assign bits 6 to 11 as the second section of the address would have

been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant.

Method claim 8 is rejected using the same rationale as for the rejection of claim 1 above.

As in claim 10, Becker teaches that a memory read command may be output directly via a fast path, and that a memory read command may alternatively be transferred to a memory read command queue (Fig. 5a, elements 94, 152 and "FAST"; column 15, line 50 to column 16, line 2).

As in claim 11, Becker teaches a flag for permitting execution of the memory read command after the memory read command is received and when the comparison between the read and write addresses indicates a difference (Fig. 5a, "RAMTCH"; column 11, line 67 to column 12, line 35). It is noted that Becker teaches de-asserting the flag when a comparison indicates a difference, however, the use of positive and negative meanings for signals are well known in the art, and one of ordinary skill in the art would recognize that the de-assertion of a signal is equivalent to the assertion of its opposite meaning. Therefore, it would have been obvious to raise a flag when the comparison indicates a difference in the system of Becker, Mills and Pollak.

9. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 1 above, and further in view of Mann (US 5,954,813).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 1 as above.

The combination of Becker, Mills and Pollak does not teach the following limitations required by claims 2-3:

a first and second compare unit coupled to the bus interface unit for receiving the first and second section read addresses, respectively, and comparing the first and second section read addresses to the identical bit portions of each write address of the memory write commands inside the memory write command queue, and outputting a first and second comparison signal; and

a grant decision unit coupled to the first and second comparison units, wherein a grant execution signal is set if either compare unit indicates a difference, otherwise the grant execution signal is set only after the memory write command with identical address bits executes.

Referring to the rationale for the rejection of claim 1, it is noted that Becker, Mills and Pollak teach the comparison of a read address against the write addresses in a memory write command queue, and granting execution of the read command if there is no match, and delaying execution of the read command until the matching write command executes if there is a match.

However, Becker, Mills and Pollak do not teach the specific configuration of the comparison function enumerated above, particularly the use of two compare units and a grant decision unit.

Mann teaches the comparison of an address divided into a first and second section against a stored address using two comparators (i.e. compare units), where a control unit (i.e. grant decision unit) receives the results of the comparison from each comparator and outputs a signal (i.e. grant execution signal) to allow the continued execution of a process if the addresses do not match, and halt execution of a process if the addresses match (Fig. 3; column 3, lines 47-55; column 6, lines 11-52).

Regarding claims 2-3, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the address comparison configuration taught by Mann to execute the address comparison function in the system made obvious by the combination of Becker, Mills and Pollak, as suggested by the similarity in the nature of the problem to be solved which would have been recognized by one of ordinary skill in the art at the time of the invention.

Regarding claim 3, the rationale derived from Becker in the rejection of claim 10 above is incorporated herein for the teaching that a memory read command may be output directly via a fast path, and that a memory read command may alternatively be transferred to a memory read command queue.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 1 above, and further in view of applicant's admitted prior art (APA).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 1 as above.

The combination of Becker, Mills and Pollak does not teach that transfer of the first section read address requires two bit times, where a rising edge and a falling edge of the clock are both defined as a bit time, as required by claim 4.

APA describes a system bus defined by AMD Corporation where each rising and falling edge of the clock signal is defined to be a single bit time unit and the first section read address is transmitted in two bit time units (Page 4, paragraph 9).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to define each rising and falling edge of the clock signal to be a single bit time unit, and to require two bit time units to transfer the first section read address, in the system made obvious by the combination of Becker, Mills and Pollak, as suggested by the applicant's own admitted prior art.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 8 above, and further in view of applicant's admitted prior art (APA).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 8 as above.

The combination of Becker, Mills and Pollak does not teach that transfer of the first section read address requires two bit times, where a rising edge and a falling edge of the clock are both defined as a bit time, as required by claim 9.

The rationale set forth in the rejection of claim 4 is applied herein for the rejection of claim 9.

Response to Arguments

12. Applicant's arguments filed 5 February 2004 with respect to the rejection of claims 1 and 8 under 35 USC 103(a) have been fully considered but they are not persuasive.

Applicant asserts that there is no suggestion to combine Becker and Mills with Pollak because Becker and Mills teach using an address as a single unit and therefore teach away from using the address in several parts (Amdt. A, pages 11-12).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art (see MPEP § 2143.01).

In this case, Becker teaches a comparison involving an address, which may be viewed as a unitary collection of bits. Pollak teaches a comparison involving a string, which likewise may be viewed as a unitary collection of bits. The similar nature of the problems to be solved would suggest to one of ordinary skill in the art to use the comparison method of Pollak for the address comparison in the system of Becker.

Pollak further teaches a comparison method where characters of the string (i.e. divided units) are sequentially compared, and that the sequential comparison is terminated upon the first mismatch (Pollak, Fig. 2 and column 4, lines 18-39). It is clear in Pollak that terminating the comparison upon the first mismatch produces the same result in less time than if the entire string were compared (Pollak, column 1, line 66 to column 2, line 4). Thus, where the comparison method of Pollak is used for the address comparison of Becker, one of ordinary skill in the art would be motivated to carry out a subsequent comparison on a second section of the address only if the comparison on a first section of the address resulted in a match.

Applicant further asserts that the combination of Becker and Mills does not teach a two-step comparison algorithm performed before the row and column address are combined (Amdt. A, page 12).

Examiner points out that the two-step comparison algorithm of the address is derived from the teachings of Pollak in combination with Becker and Mills. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furthermore, claims 1 and 8 do not recite the limitation that the comparison is performed before the address is combined. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

13. Applicant's arguments filed 5 February 2004 with respect to the rejection of claims 2 and 3 under 35 USC 103(a) have been fully considered but they are not persuasive.

Claims 2 and 3 are rejected over the combination of Becker, Mills, Pollak and Mann. Applicant reasserts arguments presented with regard to claims 1 and 8 that Pollak cannot be combined with Becker and Mills, then proceeds to assert that the combination of Becker, Mills

and Mann, absent Pollak, do not disclose to first compare the first section address and then compare the second address if it is necessary (Amdt. A, pages 13). The arguments asserting that Pollak cannot be combined with Becker and Mills were found to be unpersuasive in the response to arguments related to claims 1 and 8 above. Therefore, these arguments are also unpersuasive as applied to claims 2 and 3.

Applicant further asserts that Mann does not teach the aforementioned comparison algorithm (Amdt. A, page 14). Applicant is reminded that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.

14. Applicant's arguments filed 5 February 2004 with respect to the rejection of claims 4 and 9 under 35 USC 103(a) have been fully considered but they are not persuasive.

Applicant's arguments follow the same reasoning as in the arguments with respect to claims 1-3 and 8 that were found to be unpersuasive in the response to arguments above. In particular, Applicant reasserts that Pollak cannot be combined with Becker and Mills, and further asserts that neither Becker combined with Mills, nor APA teach a two-step comparison algorithm. For the same reasons stated above, these arguments are also unpersuasive as applied to claims 4 and 9.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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